ABSTRACT OF THE DISCLOSURE

An apparatus for serial data communication between a plurality of IC chips with a reduced number of inter-chip signal lines. In the apparatus, one IC chip acts as a master, while the other chip(s) are slaved to it. In response to conditions internal to the master chip or in response to a request from at least one of the slave chips, the master chip generates a transfer control signal and a synchronization clock signal. The transfer control signal defines a transfer phase during which data transfer among the chips can take place. The chips take turns sending and receiving data in a multiplexed fashion, with sending and receiving parties designated by a count of synchronization clock signal cycles. The synchronization clock signal is generated at a high frequency, to allow fast data transfer.